

The diagram illustrates a High-speed serial data interface with two channels, A-ch and B-ch. Channel A (A-ch) consists of a receiver section (RXA) and a transmitter section (TXA). The receiver section includes a differential input (DINA) connected to a pair of input lines (3A) which feed into a PI (Phase Interpolator) and CDR (Charge Pump and Frequency Divider) block. The output of this block is connected to a pair of lines (5A) which feed into a Des (Deserializer) block. The Des block has two output lines (7A) connected to a receiver block (RDA). The transmitter section includes a Ser (Serializer) block that receives data from a TXA input and outputs it to a transmitter block (TDA). Channel B (B-ch) is similar but uses different signal names: RXB, DINB, 3B, 5B, 7B, Des, RDB, TXB, and DOUTB. The central TDA and TDB blocks are connected to the Ser blocks of both channels. The entire interface is labeled 'High-speed serial data interface' at the bottom.

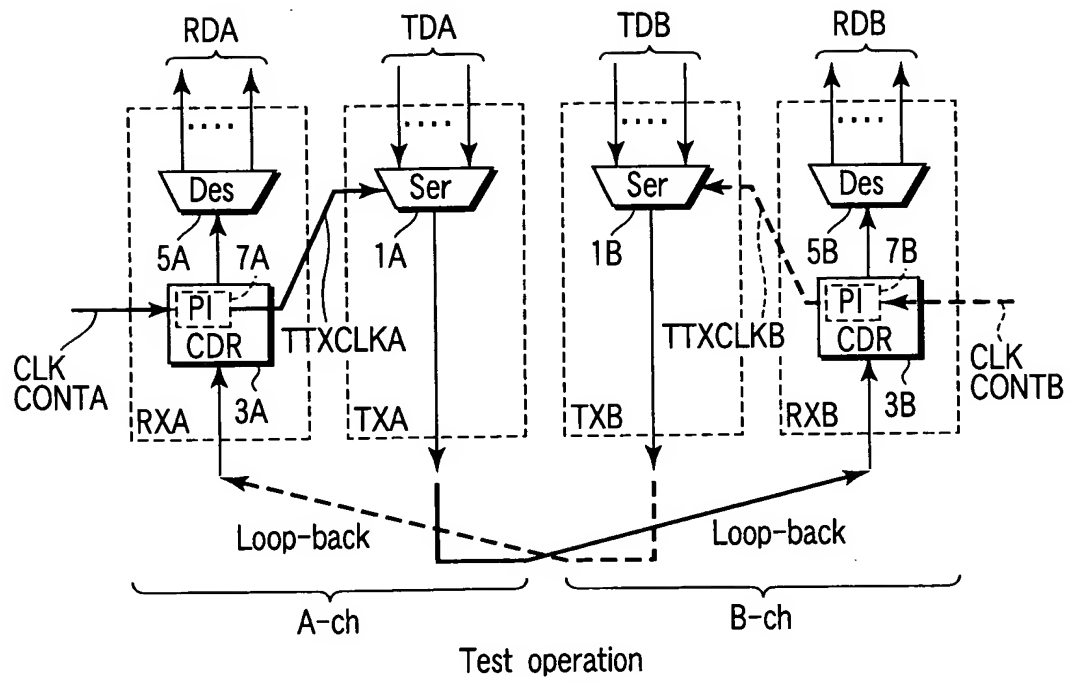
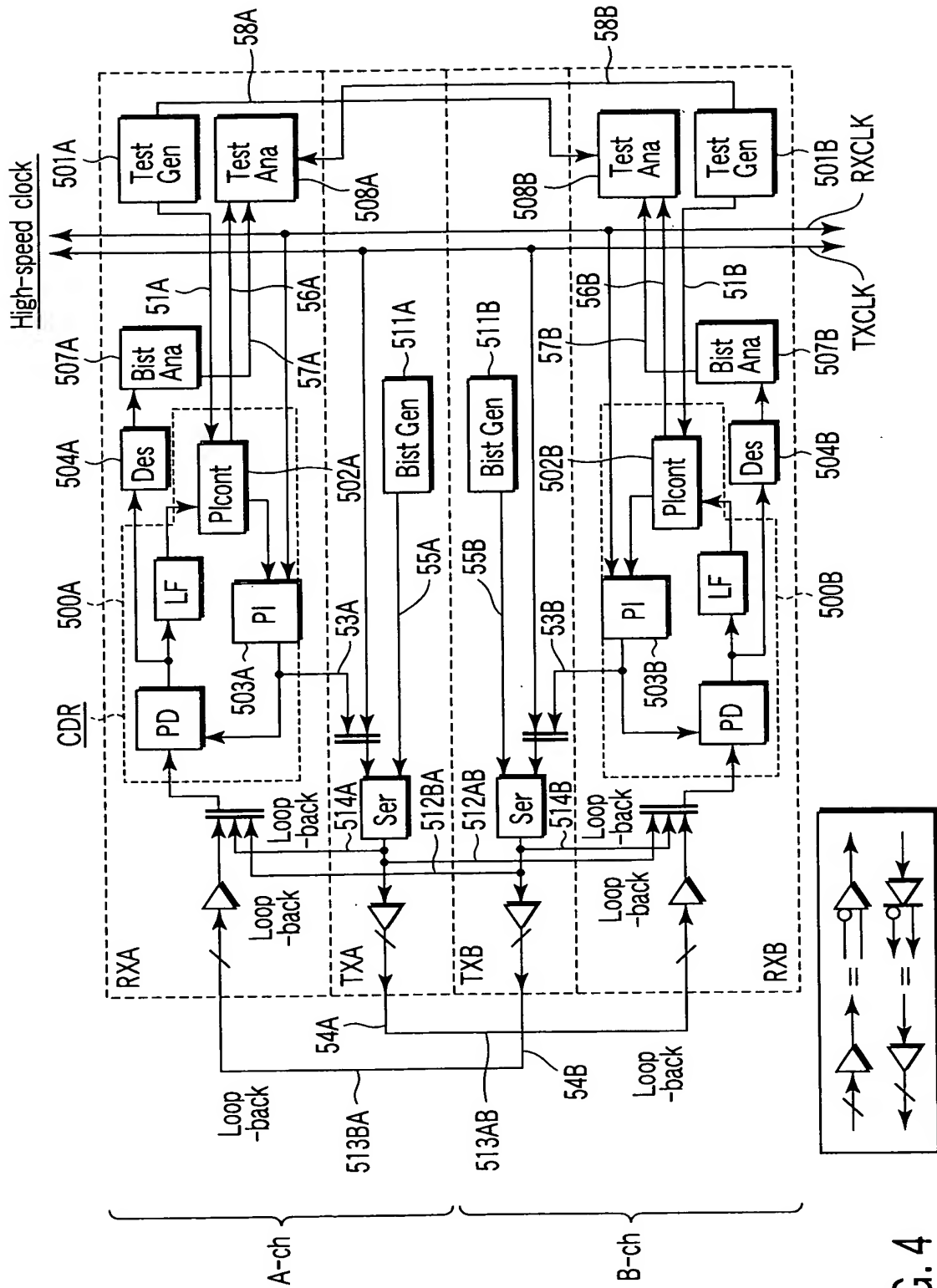


FIG. 3



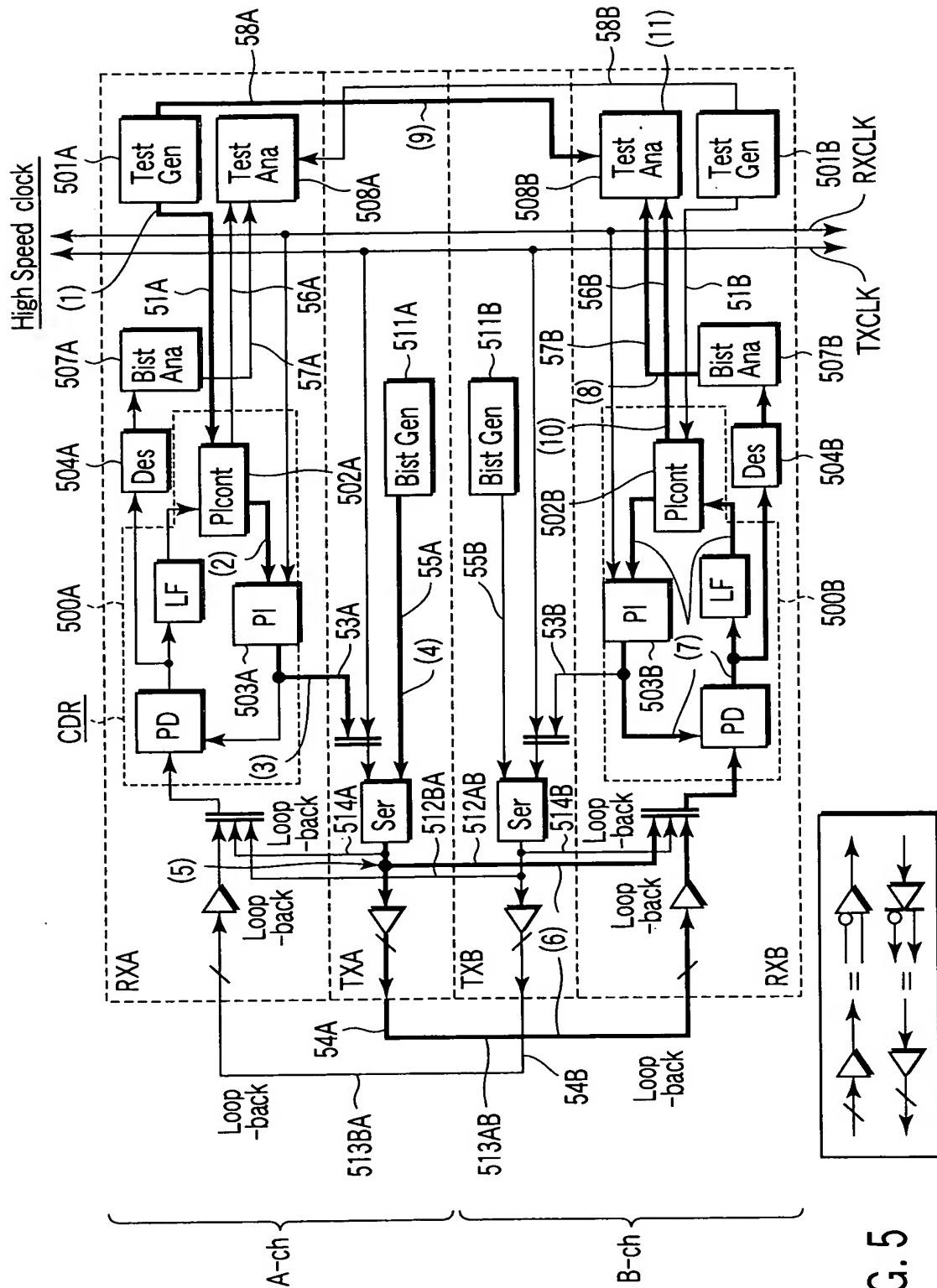


FIG. 5

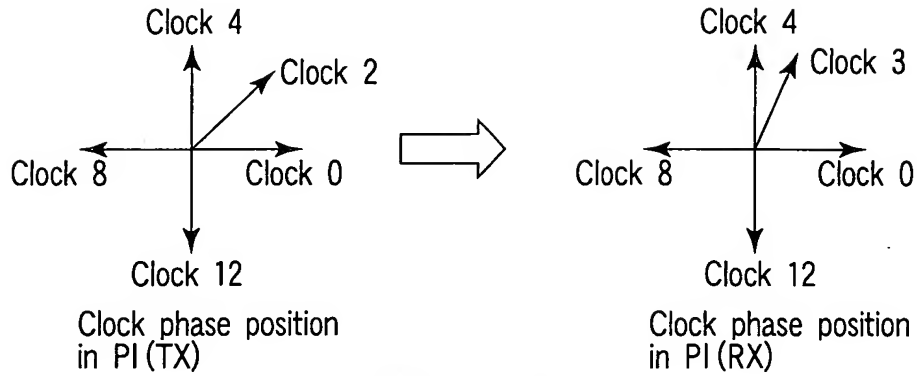


FIG. 6

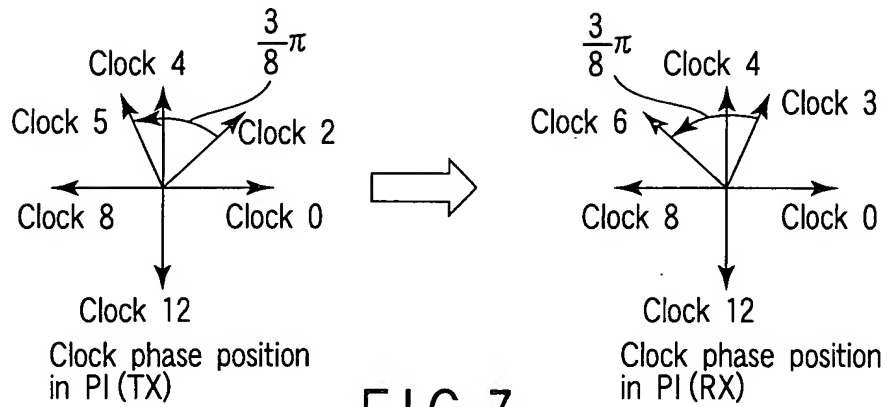


FIG. 7

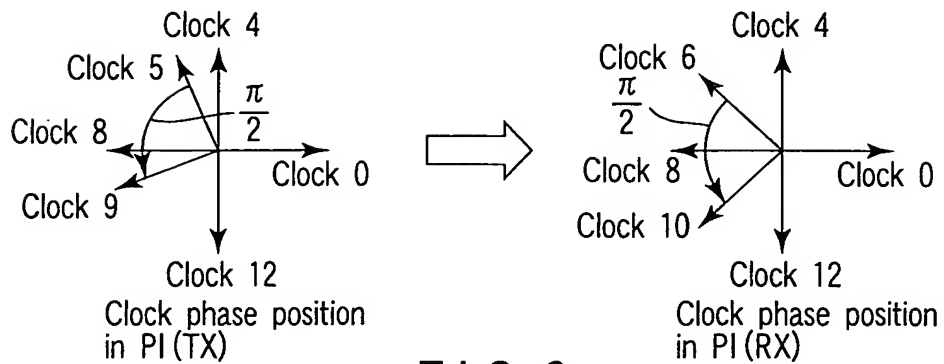
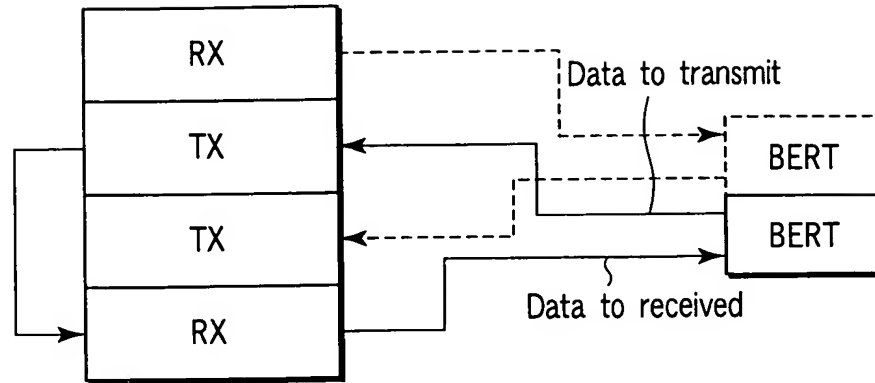


FIG. 8



Bit error rate testing

FIG. 9

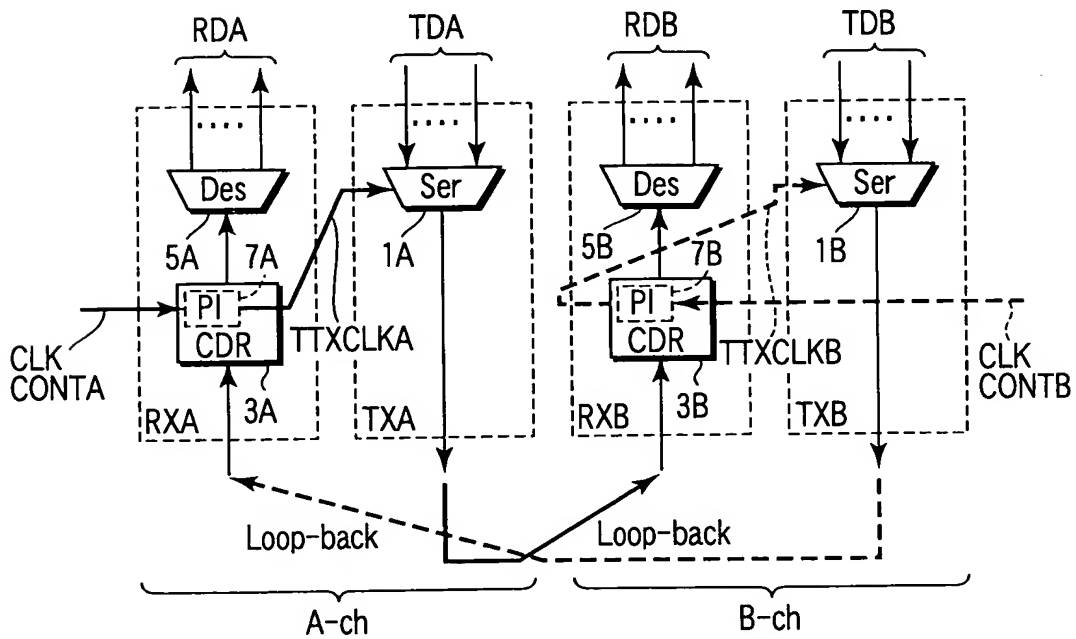


FIG. 10

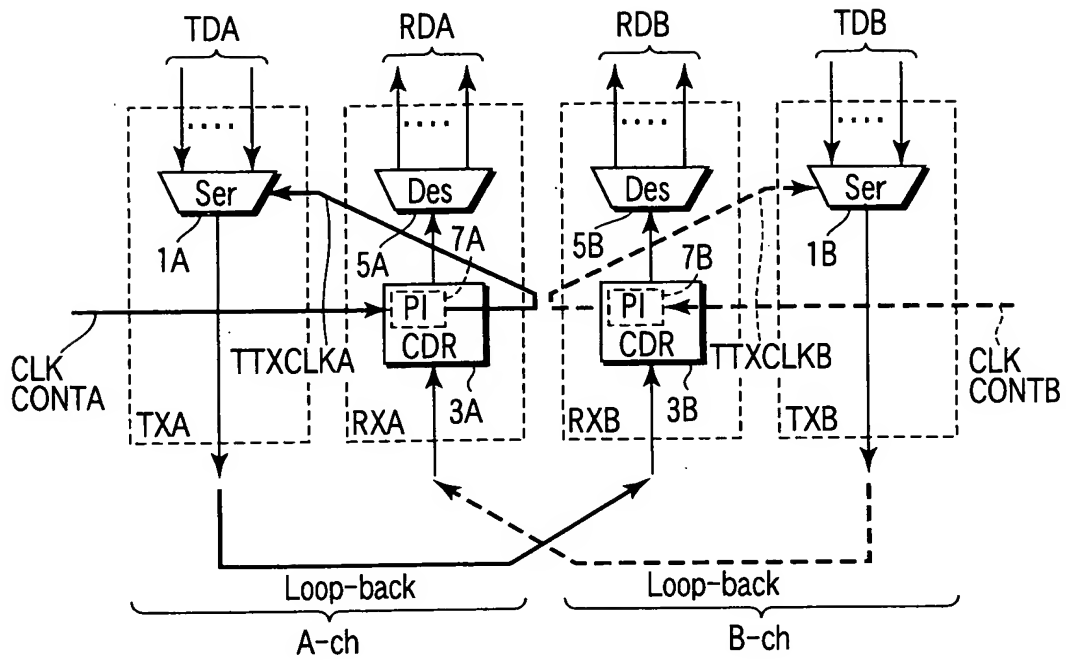


FIG. 11

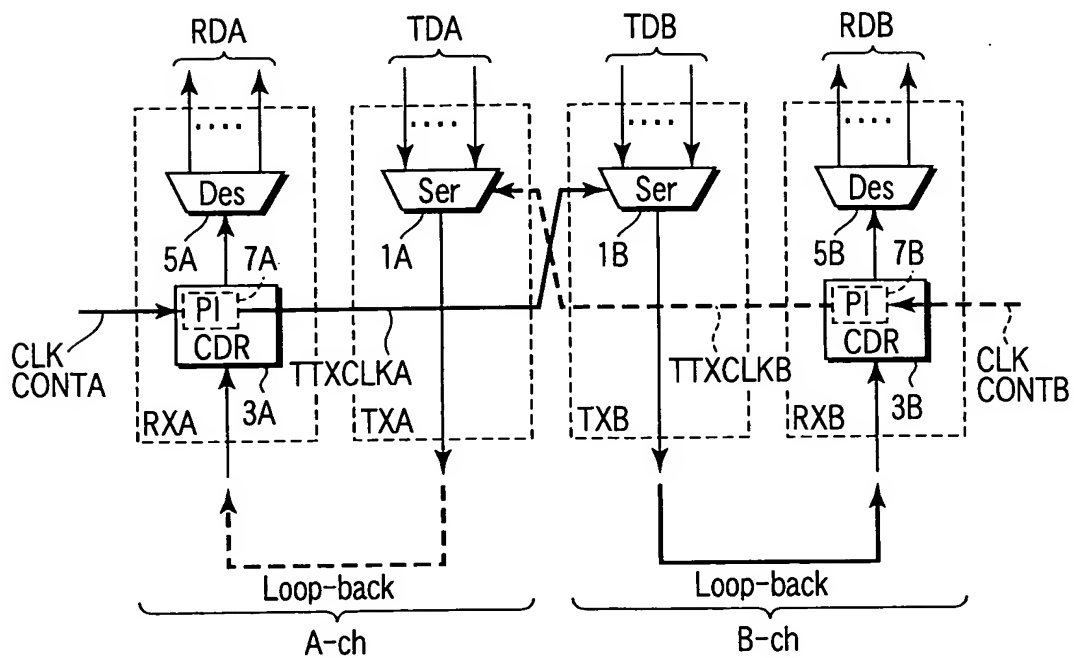


FIG. 12

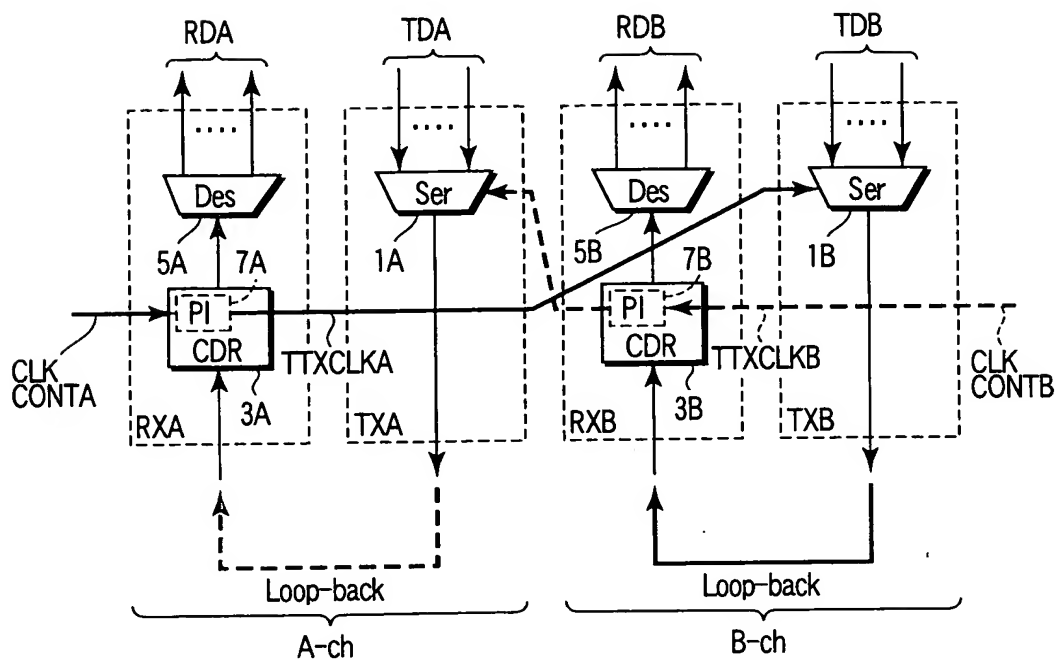


FIG. 13

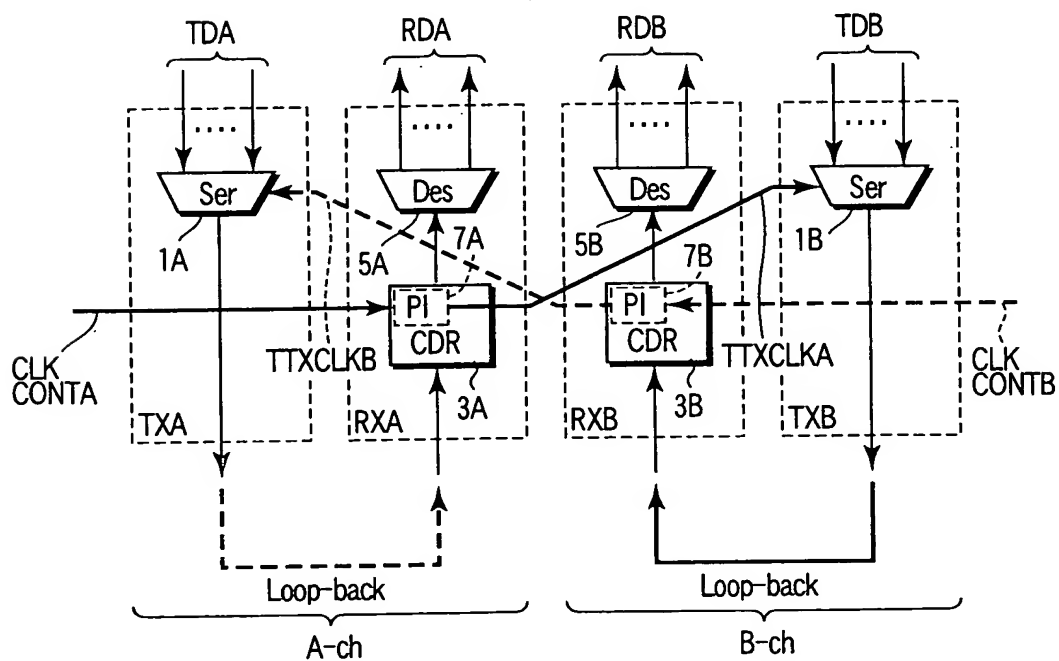


FIG. 14



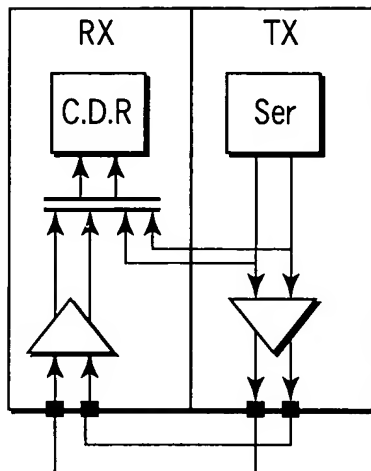


FIG. 15 PRIOR ART

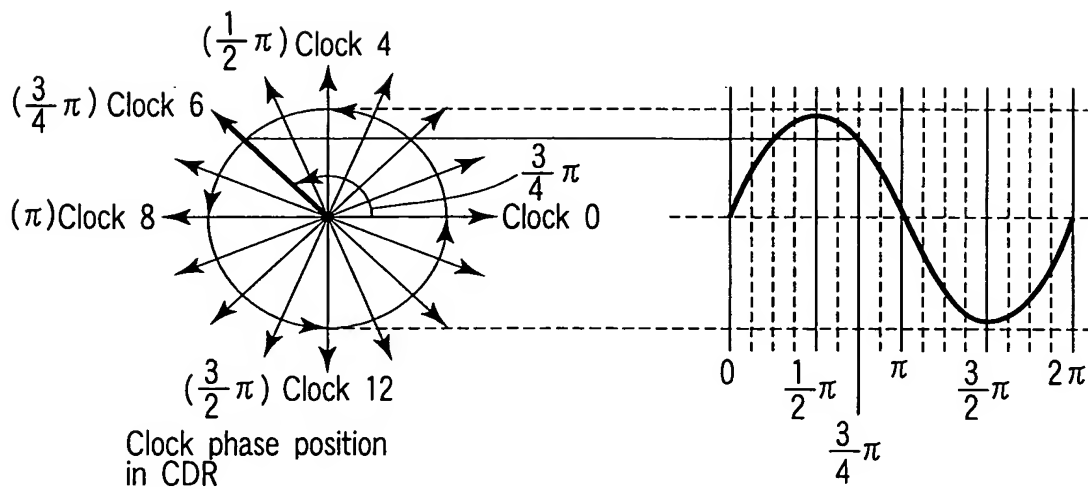


FIG. 16 PRIOR ART

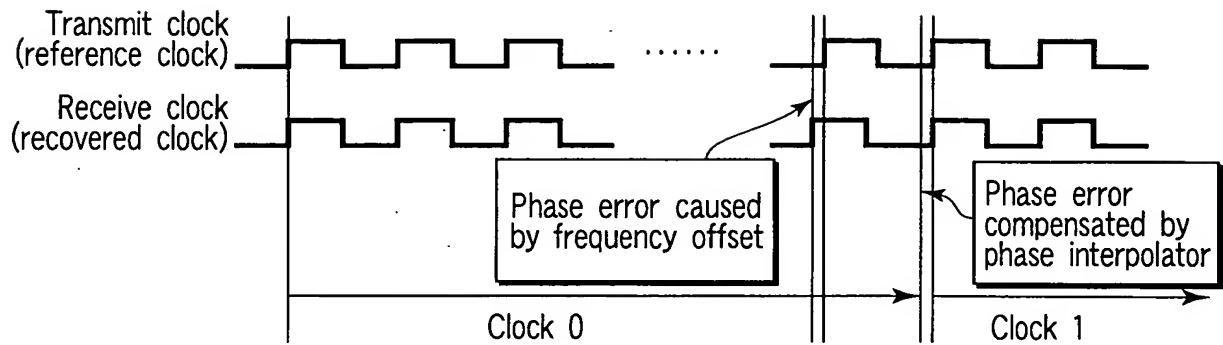


FIG. 17 PRIOR ART

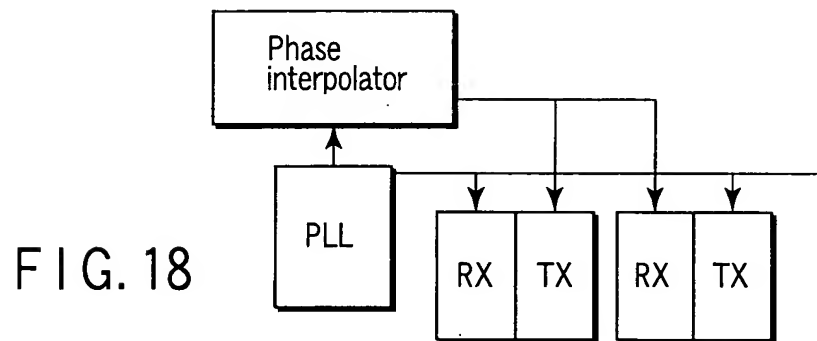


FIG. 18

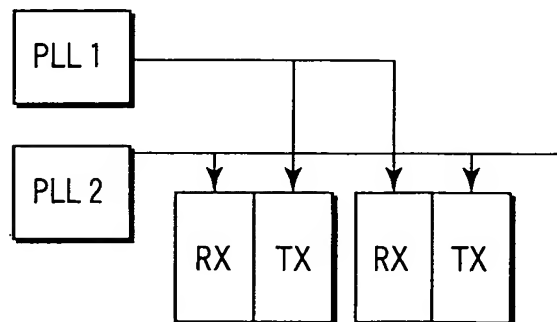


FIG. 19